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Direct Growth and Patterning of Multilayer Graphene onto a Targeted Substrate without an External Carbon Source

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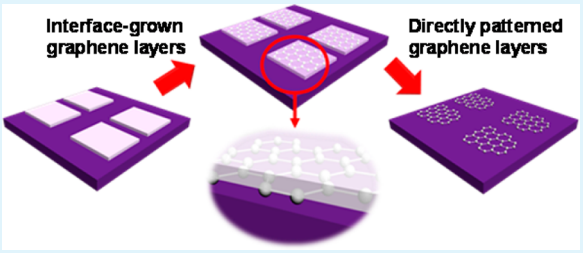
ABSTRACT: Using only a simple tube furnace, we demonstrate the synthesis of patterned graphene directly on a designed substrate without the need for an external carbon source. Carbon atoms are absorbed onto Ni evaporator sources as impurities, and incorporated into catalyst layers during the deposition. Heat treatment conditions were optimized so that the atoms diffused out along the grain boundaries to form nanocrystals at the catalyst-substrate interfaces. Graphene patterns were obtained under patterned catalysts, which restricted graphene formation to within patterned areas. The resultant multilayer graphene was characterized by Raman spectroscopy and transmission electron microscopy to verify the high crystallinity and two-dimensional nanomorphology. Finally, a metal−semiconductor diode with a catalyst−graphene contact structure were fabricated and characterized to assess the semiconducting properties of the graphene sheets with respect to the display of asymmetric current−voltage behavior.



KEYWORDS: *graphene, interface growth, external carbon source*

1. INTRODUCTION

With its fascinating properties, including an ultrahigh carrier mobility and nonlinear optical effects, graphene has attracted widespread attention as a promising emerging enabler of future electronic and optoelectronic devices.[1,2] Numerous approaches have been developed in an effort to achieve the universal goals of high-efficiency graphene synthesis and improved nanostructural and electrical properties, such as crystallinity, carrier mobility, and crystal scalability.[3−7] Elegant applications, including graphene-based transparent electrodes, active device channel layers, battery electrodes, graphene-assisted femtosecond lasers, and photodetectors, have been intensively studied, yielding promising results within a very short period of time.[2,8−12] Unfortunately, the contact resistance between nanolayers and the control over the morphology and layer numbers in multilayer graphene has remained a substantial roadblock to the development of future electronics and to photonic applications. A reproducible solution to the problem of transferring graphene onto a customized substrate is required to escape the deleterious defects on and within nanostructures and to improve the efficiency of device fabrication. Recent reports have described multilateral trials that simplify the preparation of graphene-based devices.[13−16] A smart approach to forming graphene layers between a substrate and catalyst has been developed to avoid the transfer process. Here, polymer materials as carbon sources were sandwiched between catalyst and substrate layers and were burned to supply carbon atoms and to control the local carbon concentration at the interlayer zone for the direct formation of graphene layers on the designed substrate. Although the 'interlayer growth' technique has opened a new phase of research in the field of graphene synthesis methods, carbon source feeding remains a critical problem because polymer carbon sources can cause uncontrollable defect formation in a nanolattice, poor crystal uniformity, and pollution problems.[16−19] Moreover, the patterning of graphene layers using a polymer carbon source is challenging without the removal of the polymer layers deposited onto the unpatterned areas.

In this work, we demonstrate the formation of patterned multilayer graphene at the interlayer between a catalyst and a substrate without employing an external carbon source. A tube furnace was used as the main equipment for synthesis. Carbon atoms were supplied from the surroundings as impurities that diffused into the Ni catalyst, in which carbon was significantly soluble,[17,20] and the carbon atoms then diffused back out to its surface during heat treatment to engage in crystal formation. The conditions of crystal nucleation and growth were optimized to synthesize graphene layers at the catalyst−substrate interlayer rather than at the top surface of the catalyst. Because graphene formation was restricted to the catalyst area, patterning of the resultant graphene was achieved simply by patterning the catalyst. The patterned multilayer graphene was investigated by Raman spectroscopy and transmission electron microscopy (TEM) to verify the successful formation of few-layer structures within the patterned area. A metal−semiconductor (MS) diode was

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fabricated using the prepared graphene and Ni catalyst layers to characterize the semiconducting properties of the graphene.

2. EXPERIMENTAL SECTION

The graphene layer was synthesized using a tube furnace that did not require source feeding equipment, rather than using chemical vapor deposition (CVD) methods, which are conventional tools for the preparation of relatively large high-quality graphene. We developed an "interlayer growth" technique that guaranteed the efficient preparation and patterning of graphene between the substrate and catalyst layers so that transfer processes could be avoided. We emphasize that the carbon atoms were not supplied from an external carbon source but originated from ambient impurities that included carbon atoms and could be hosted by the Ni catalyst. Schematic diagrams of the entire process are depicted in Figure 1.

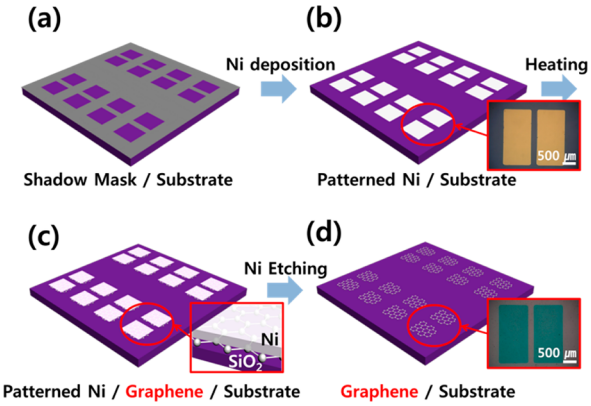

Figure 1. Conceptual explanation of the experimental procedure for patterned interlayer growth of graphene without source feeding. Ni was employed as the catalyst. Simple catalyst patterning guaranteed cloning of the pattern in the graphene layer.

Nickel and a 300 nm SiO_2/Si wafer were used as the catalyst and substrate, respectively. The substrate was cleaned with piranha solution (H_2SO_4:H_2O_2 = 10:7) to remove organic contaminants. The patterned graphene was obtained by applying a shadow mask to the substrate for Ni deposition (see Figure 1a), and 100 nm of a Ni film was deposited on the substrate using an electron beam (e-beam) evaporator (SNTEK MEP5000, see Figure 1b). The as-deposited sample was heated at 1000 °C for 40−50 s under a vacuum of 1×10^{-3} Torr. The sample was then cooled to room temperature within 3−4 min to permit nucleation and growth of the graphene crystals (see Figure 1c). Finally, Ni was etched away using a 0.1−0.2 M $FeCl_3$ solution (see Figure 1d), yielding the patterned multilayer graphene. The Raman spectrum of the synthesized graphene was collected to ensure the successful formation of multilayered nanocrystals. The formation of interlayer nanosheet structures only between the catalyst and the substrate was confirmed using an FEI NOVA Nano 200 scanning electron microscope (SEM), FEI Tecnai F20 G^2 transmission electron microscopy (TEM) operated at 200 kV. For the graphene transfer to TEM grid, catalyst-etched graphene/SiO_2/Si sample was floated on buffered oxide etchant for the SiO_2 etching. After its separation from the substrate, graphene was floated and scooped with a copper grid together.

3. RESULTS AND DISCUSSION

SEM images of the e-beam-evaporated catalyst layer before and after thermal treatment are shown in images a and b in Figure 2, respectively.

The polycrystalline morphology of the catalyst played a critical role in determining both the morphology and crystallinity of the resultant graphene. Without heat treatment, the catalyst showed a small uniform grain distribution,

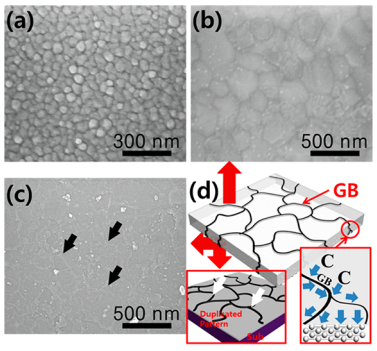

Figure 2. SEM images used for surface characterization of the catalyst (a) before and (b) after thermal treatment, and (c) surface morphology of the resultant graphene. (d) Proposed GB diffusion mechanism for carbon atoms hosted in the catalyst matrix.

illustrating poor grain growth and a high density of grain boundaries (GBs). On the other hand, as shown in Figure 2b, large grains of nickel, 500 nm in diameter, were obtained after the high-temperature heat treatment. The grain size could be adjusted by optimizing the treatment conditions, such as multistepping the thermal treatment (the first step is for the control of the grain size, and the second step is for the graphene synthesis) to control the GB density, which determined the flux of carbon atoms out of the catalyst layer and managed the rate of nucleation and growth of graphene. SEM images of the synthesized graphene layer are shown in Figure 2c. The duplicated weak patterns of Ni-GB on the graphene layer verified the high carbon density near the GBs (see Figure 2d) and the high-speed diffusion paths for the carbon atoms. Thus, GB diffusion played a major role in the carbon supply and the formation of atomic layered crystal structures. The electrical properties of graphene, which depend on the grain size, can be tuned by controlling the Ni grain size as well.[21]

The TEM images shown in Figure 3 depict the synthesized multilayer graphene, which was verified by characterizing the

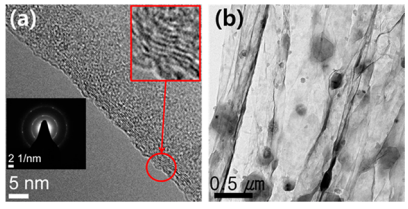

Figure 3. (a) TEM image of multilayer graphene. The insets show the SAED patterns and edge-magnification. (b) Wide view of a TEM image showing additional graphene plates on the primary graphene sheet.

folded edge (see the inset of Figure 3a). We observed 5−10 layers of stacked graphene. We also obtained selected area electron diffraction (SAED) patterns of the nanosheets, as shown in the inset of Figure 3a. Clear hexagonal patterns with bright spots were observed, indicating that the graphene had well-defined 6-fold symmetry. SAED pattern shows 'arcs' feature indicating the presence of rotational stacking faults in the multilayer graphene. This explains the higher 2D peak even though it is not single layered graphene. Irregular hexagons formed additional layers on the graphene sheet, as can be seen in Figure 3b. The equivalent dimensional scaling between the Ni grains and the interlayer distances between the additional

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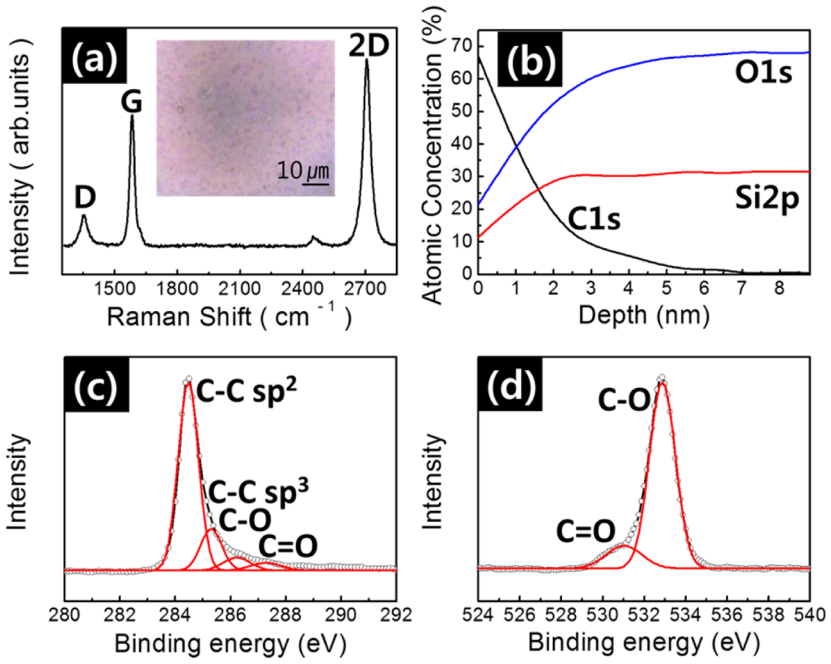

Figure 4. (a) Raman spectrum of graphene synthesized on a 300 nm SiO_2/Si substrate. The inset shows the optical microscopy image of the sample used for Raman analysis. XPS data for the graphene on an identical substrate used for (b) depth profiling, and spectra containing multiple subpeaks around the (c) C1s peak and (d) O1s peak obtained from Gaussian fit.

layers suggests a possible explanation for the role of GBs in providing carbon delivery pipes and nucleation sites yielding a high carbon density.

The synthesized graphene layers were characterized by Raman spectroscopy, as shown in Figure 4(a). Our multilayer graphene layers on the SiO_2/Si substrates exhibited a typical graphene spectrum with two intense peaks at 2706 cm^{-1} (2D peak, I = 4948) and 1584 cm^{-1} (G peak, I = 3866). Even though a considerable 2D peak has single Lorentzian line shape and narrow full width at half-maximum (36 cm^{-1}) that imply the formation of singlelayer graphene, Raman shift detected at 2706 cm^{-1} explains the formation of few-layer graphene, which is in accordance with the result from the TEM analysis.[19] (see Figure 3a). The defects that perturbed the graphene lattice resulted in a weak D peak at 1352 cm^{-1} with the D/G ratio of 0.237, and the ration can be improved by optimizing the process condition. The inset in the figure illustrates the uniform morphology of the graphene sheet observed by optical microscopy. X-ray photoelectron spectroscopy (XPS) was employed to investigate the compositional profile of the sample. The main components of the samples included C1s and a part of O1s detected from the graphene layer, and the most part of O1s and Si2p originated from the substrate. Figure 4b supports the formation of graphene directly on the substrate confirming the highly biased existence of nanoscaled carbon atoms with the surface concentration of 67.84%. The C1s (see Figure 4c) and O1s (see Figure 4d) XPS peaks were decomposed into Gaussian subpeaks corresponding to the presence of C−O and C═O bonds and disordered regions in the graphene lattice.[22−27] The weight percent of nonoxidized carbon was found to be about 88% from the C1s and O1s spectra. Because the Si2p levels and partial O1s levels were detected originally from the SiO_2 substrate, the carbon content of the top surface of the graphene sheet was expected to be higher than the measured value.[28] This result was supported by the ratio C−C/C−O/C═O, as shown in Figure 4c.

To analyze the surface morphology of the synthesized graphene layer, atomic force microscopy (AFM) was employed. Images a and b in Figure 5 describe the three-dimensional

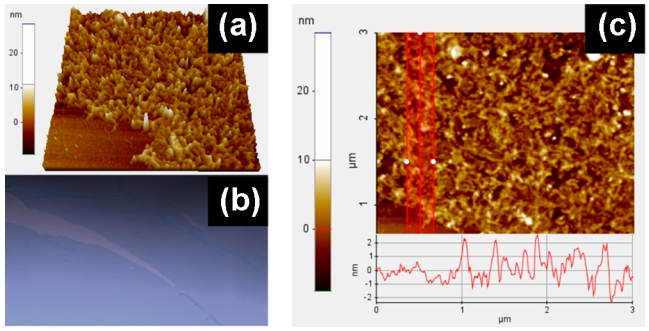

Figure 5. AFM data for the surface morphology of the graphene layer including (a) three-dimensionally visualized graphic, (b) image from optical microscope, and (c) thickness data.

graphic of the graphene layer and the image from optical microscope, respectively. In the figures, the graphene layer and substrate can be clearly discriminated; therefore, the formation of the graphene layer was ensured. The thickness of the graphene layer can be estimated with the data shown in Figure 5c. The measured results represented that the average thickness is less than 2 nm.

The semiconducting properties of the graphene sheet synthesized by the interlayer growth method were verified by constructing and investigating a Schottky diode with a metal−semiconductor (MS) contact. An as-deposited Ni catalyst (in which the work function of Ni was 5.15 eV) was used as the metal to avoid additional metal deposition steps. After graphene synthesis at the interlayer, the Ni catalyst was partly etched so that the graphene layer could display both MS contacts and opened areas. The device structure is described in the inset of

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Figure 6. As shown in Figure 6, an asymmetric $I-V$ curve (bias-dependent conducting characteristics) was obtained at

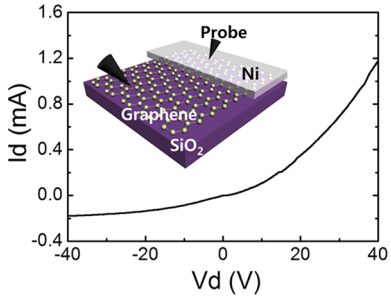

Figure 6. Asymmetric $I-V$ characteristics of the graphene-based MS diode. The inset shows the device structure with the graphene sheet and Ni layer that formed the semiconductor−metal contact structure.

considerable current levels. The defects and irregularities introduced into the graphene layer during the process, however, formed multiple parallel current paths that rounded up the turning point of the curve. The defects provided conduction barriers in the form of serial resistance components with the threshold voltages higher than 10 V.

4. CONCLUSION

Using only a simple tube furnace, we demonstrated the direct synthesis of graphene on a designed substrate without the use of external carbon source. Impurities supplied by the surroundings were absorbed onto the surface of Ni source and the substrate, and carbon atoms were introduced into the catalyst matrix during the deposition. By heat treatment, the carbon atoms diffused out to form the 2-dimensional crystals at the catalyst-substrate interface. Patterned graphene was obtained using a simple patterned catalyst, which restricted the growth area within the catalyst patterns. This approach provides a new processing paradigm for the preparation of graphene and graphene-based devices for use in future high-performance applications. The method used simple efficient equipment that did not require a source feeding setup.

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Notes

The authors declare no competing financial interest.

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